DMT040H8HMCMI-1A
PRODUCT SPECIFICATION

Version 0.1
Feb 01, 2021

Customer's Approval	
Signature	*Date*

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Approved by *Eric Wan*

Revision History

VERSION	DATE	DESCRIPTION	AUTHOR
0.1	Feb 01, 2021	Preliminary	Joyce Huang

Legal Notice

Table of Contents

1. General Description

1.1 Introduction

This is a 4” size colour active matrix TFT LCD module that uses amorphous silicon TFT as a switching device. The display is normally black mode, transmissive, and featuring high contrast and excellent colour saturation. The resolution of the TFT-LCD is 720 x 720 and can display up to 16.7M colours. The display module supports 2/3/4 Lane MIPI interface and optical bonding touch panel.

1.2 Main Features

Item	Contents
Display Type	TFT LCD
Screen Size	4” Diagonal
Display Format	720 x RGB x 720 Dots
No. of Colour	16.7M
Overall Dimensions	84.00 (W) x 85.99 (H) x 4.23 (D) mm
Active Area	71.93 (W) x 71.93 (H) mm
Mode	Normally Black / Transmissive / IPS
Surface Treatment	Anti-Glare (3H)
Viewing Direction	All round
Interface	1/2/3/4 Lane MIPI
Driver IC	ST7703
Backlight Type	LED, White, 12 chips
Touch Panel	CTP
Touch Interface	I^2C
Bonding Type	Optical Bonding
Operating Temperature	-30°C ~ +80°C
Storage Temperature	-30°C ~ +85°C
ROHS	Compliant to RoHS 2.0

1.3 Touch Features

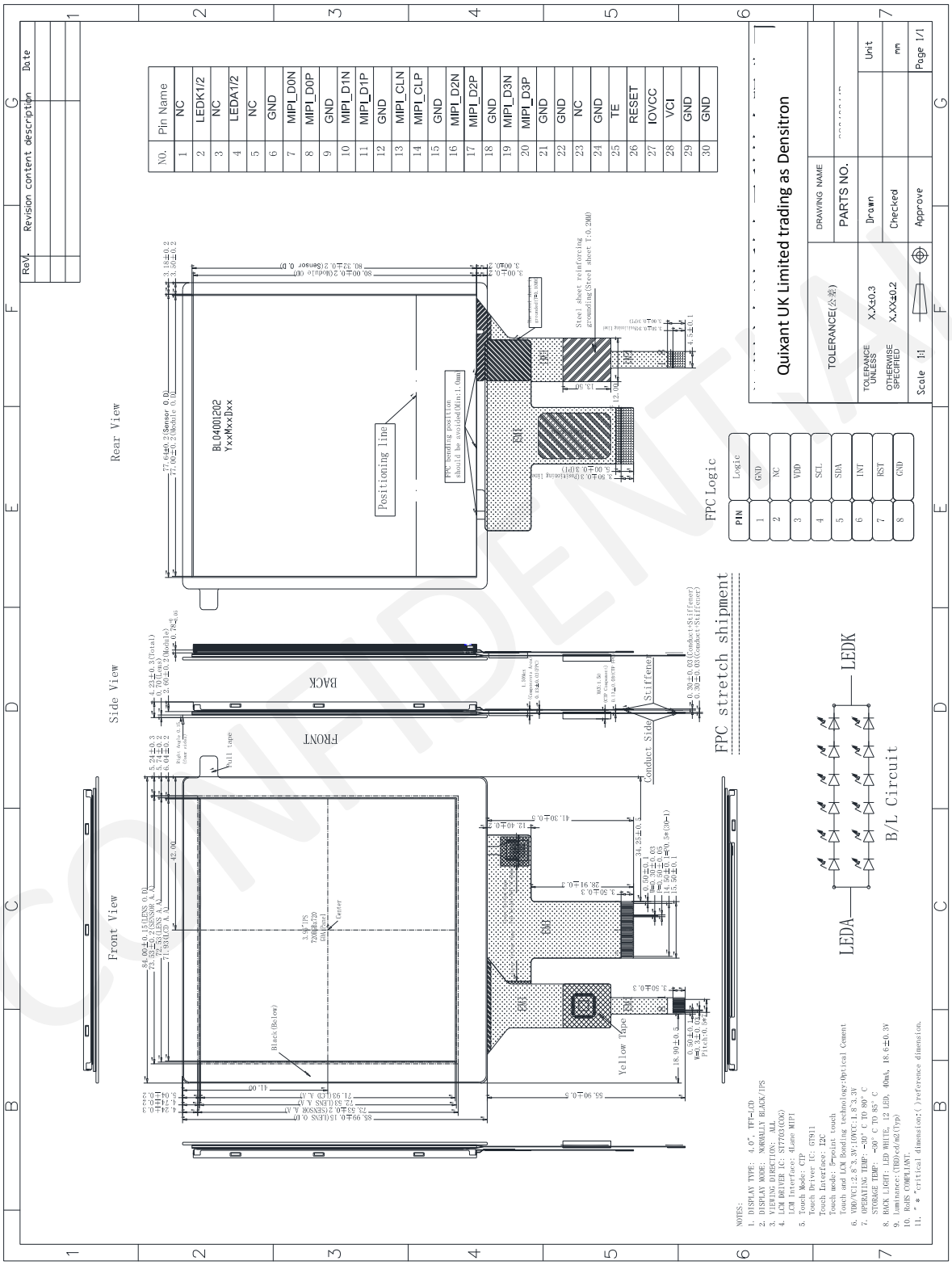
Item	Contents
Touch Panel	CTP
Structure	G+G
Touch Interface	I^2C
Slave Address	0x5D(7bit) or 0x14(7bit)
Bonding Type	Optical Bonding
CTP Driver IC	GT911
Touch mode	5 points and gestures

2. Mechanical Specification

2.1 Mechanical Characteristics

Item	Characteristic	Unit
Display Format	720 x RGB x 720	Dots
Overall Dimensions	84.00 (W) x 85.99 (H) x 4.23 (D)	mm
Active Area	71.93 (W) x 71.93 (H)	mm
Dot Pitch	0.0999 (W) x 0.0999 (H)	mm
Weight	55	g
IC Controller/Driver	ST7703	

2.2 Mechanical Drawing



3. Electrical Specification

3.1 Absolute Maximum Ratings

Item	Symbol	Min	Max	Unit	Note
Digital Supply Voltage	VCI	-0.3	+6.6	V	1
Digital Interface Supply Voltage	IOVCC	-0.3	+5.5	V	1
Operating Temperature	T_{OP}	-30	+80	°C	-
Storage Temperature	T_{ST}	-30	+85	°C	-

Note 1: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. For normal operations, it is desirable to use this module under the conditions according to Section 3.2 “Electrical Characteristics”, to avoid malfunctioning.

Note 2: Background colour changes slightly depending on ambient temperature. This phenomenon is reversible.

Note 3: Please refer to item of RELIABILITY.

3.2 Electrical Characteristics

3.2.1 DC Characteristics

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VCI	-	2.5	3.3	3.8	V	-
Digital Interface Supply Voltage	IOVCC	-	1.65	1.8	2.0	V	-
Normal Mode Current Consumption	IDD	-	-	28	56	mA	-
Level Input Voltage	VIH	-	0.7*IOVCC	-	IOVCC	V	-
	VIL	-	GND	-	0.3*IOVCC	V	-
Level Output Voltage	VOH	-	0.8*IOVCC	-	IOVCC	V	-
	VOL	-	GND	-	0.2*IOVCC	V	-

3.3 Interface Pin Assignment

3.3.1 TFT Pin Define

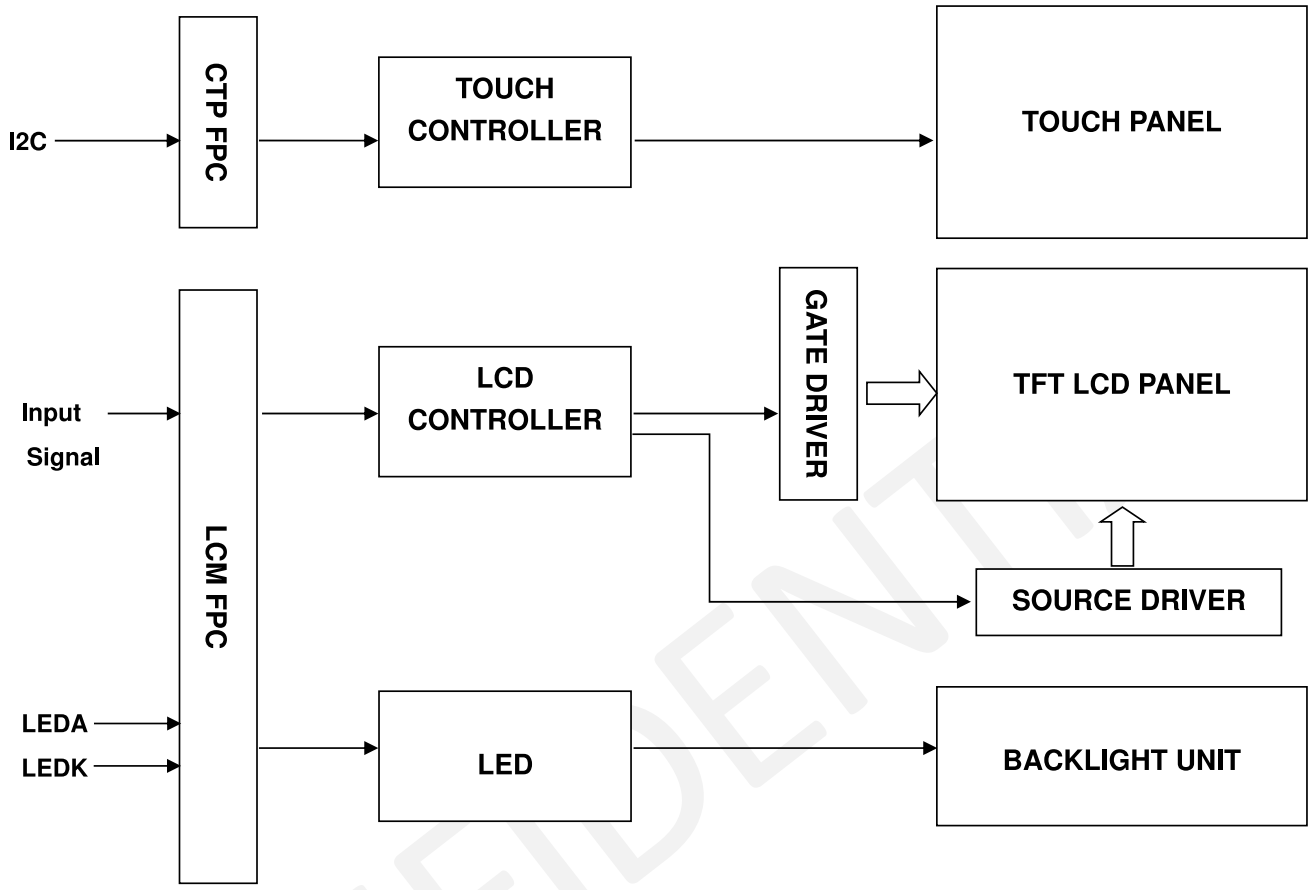
NO.	Symbol	I/O	Function
1	NC	-	-
2	LEDK1/2	P	Cathode pin of backlight.
3	NC	-	-
4	LEDA1/2	P	Anode pin of backlight.
5	NC	-	-
6	GND	P	Ground.
7	MIPI_D0N	I	- MIPI DSI differential data pair. (Data lane 0)
8	MIPI_D0P	I	
9	GND	P	Ground
10	MIPI_D1N	I	- MIPI DSI differential data pair. (Data lane 1)
11	MIPI_D1P	I	
12	GND	P	Ground
13	MIPI_CLN	I	- MIPI DSI differential clock pair
14	MIPI_CLP	I	
15	GND	P	Ground.
16	MIPI_D2N	I	- MIPI DSI differential data pair. (Data lane 2)
17	MIPI_D2P	I	Leave it to GND level when not in use.
18	GND	P	Ground.
19	MIPI_D3N	I	- MIPI DSI differential data pair. (Data lane 3)
20	MIPI_D3P	I	Leave it to GND level when not in use.
21	GND	P	Ground.
22	GND	P	Ground.
23	NC	-	-
24	GND	P	Ground.
25	TE	O	- Tearing effect output pin. Leave the pin open when not in use.
26	RESET	I	- The external reset input Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.
27	IOVCC	P	I/O power supply voltage.
28	VCI	P	Supply Voltage.

NO.	Symbol	I/O	Function
29	GND	P	Ground.
30	GND	P	Ground.

3.3.2 TP Pin Define

NO.	Symbol	I/O	Function
1	GND	P	Ground.
2	NC	-	No Connection
3	VDD	P	Supply voltage.
4	SCL	I	I^2C clock input.
5	SDA	I	I^2C data input and output.
6	INT	I	External interrupt to the host.
7	RST	I	External Reset, Low is active.
8	GND	P	Ground.

3.4 Block Diagram



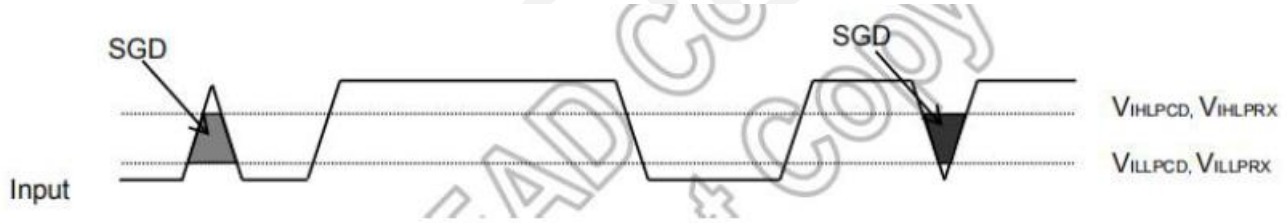
3.5 Timing Characteristics

3.5.1 DSI DC Characteristics

LP Mode

Item	Symbol	Conditions	Min	Typ.	Max	Unit
Logic high level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic low level Input Voltage	V_{ILLPCD}	LP-CD				mV
Logic high level input voltage	V_{IHLPRX}	LP-RX (CLK, D0)				mV
Logic low level input voltage	V_{ILLPRX}	LP-RX (CLK, D0)				mV
Logic low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)				mV
Logic high level output voltage	V_{OHLPTX}	LP-TX(D0)				V
Logic low level output voltage	V_{OLLPTX}	LP-TX(D0)				mV
Logic high level input current	V_{IH}	LP-CD, LP-RX				uA
Logic low level input current	V_{IL}	LP-CD, LP-RX				uA
Input pulse rejection	SGD	DSI-CLK+/-, DSI-D0+/1				Vps

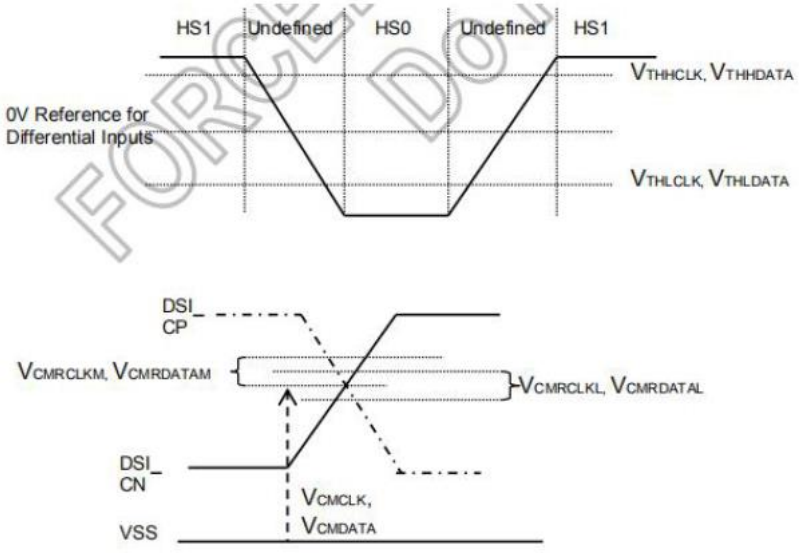
Figure: Input Glitch Rejections of Low-power Receivers



High Speed Mode

Item	Symbol	Condition	Min	Typ.	Max	Unit
Input common mode	V_{CMCLK} V_{CMDATA}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	70	-	330	mV
Input common mode variation<450MHZ	$V_{CMRCLKL}$ $V_{CMRDATAL}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-50	-	50	mV
Input common mode variation>450MHZ	$V_{CMRCLKM}$ $V_{CMRDATAM}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	100	mV
Low-level differential input threshold	V_{THLCLK} $V_{THLDATA}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-70	-	-	mV
High-level differential input threshold	V_{THHCLK} $V_{THHDATA}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	70	mV
Single ended input low voltage	V_{ILHS}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-40	-	-	mV
Single ended input high voltage	V_{IHHS}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	460	mV
Differential input termination resistor	R_{TERM}	DSI_CP/D-SI_CN DSI_D0P/DSI_D0P	80	100	125	Ω
Single ended threshold voltage for termination enable	V_{TERMEN}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	450	mV
Termination capacitor	C_{TERM}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	-	pF

Figure: Differential Voltage range and Command mode voltage



3.5.2 DSI Interface Timing Characteristics

3.5.2.1 High Speed Mode

Figure: DSI clock timing Characteristics

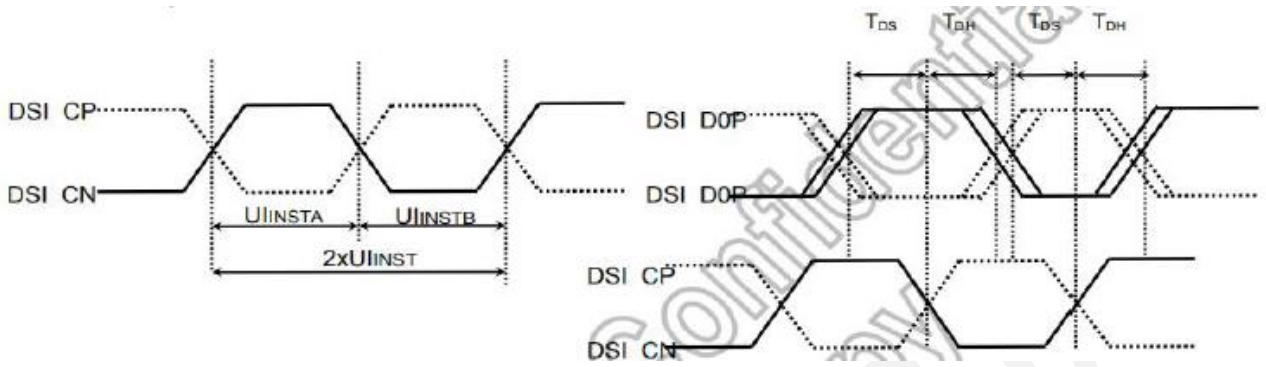


Figure: Rising and falling time on clock and data channel

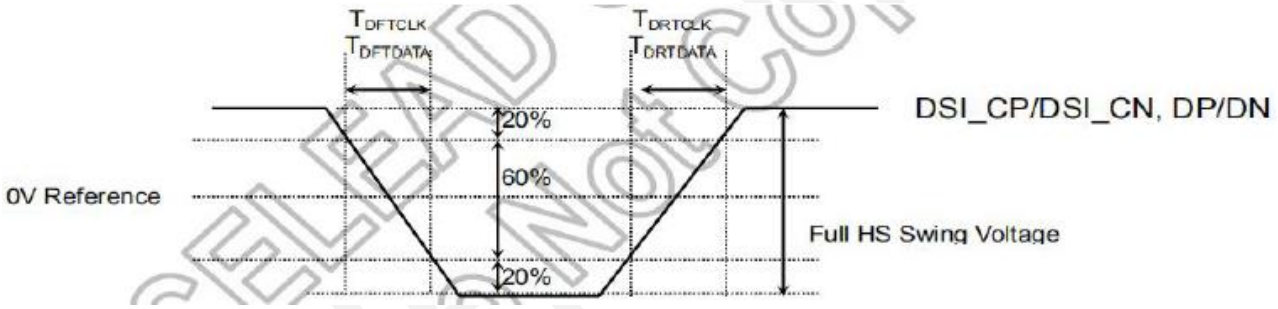


Table: DSI High Speed Mode Characteristics

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, TA=-30 to 70 ◦ C)

Signal	Item	Symbol	Min	Typ.	Max	Unit
DSI_CP/SDI_CN	Double UI instantaneous	2xUINST	TBD	-	25	ns
	UI instantaneous	UINSTA UINSTB	TBD	-	12.5	ns
DP/DN	Data to clock setup time	TDS	0.15xUI	-	-	ps
	Data to clock hold time	TDH	0.15xUI	-	-	ps
DSI_CP/DSI_CN	Differential rise time for clock	TDRTCLK	150	-	0.3UI	ps
	Differential fall time for clock	TDFTCLK	150	-	0.3UI	ps
DP/DN	Differentia rise time for data	TDRTDATA	150	-	0.3UI	ps
	Differential fall time for data	TDFTDATA	150	-	0.3UI	ps

3.5.2.2 Lower Power Mode

Figure: BTA from HOST to Display Module Timing

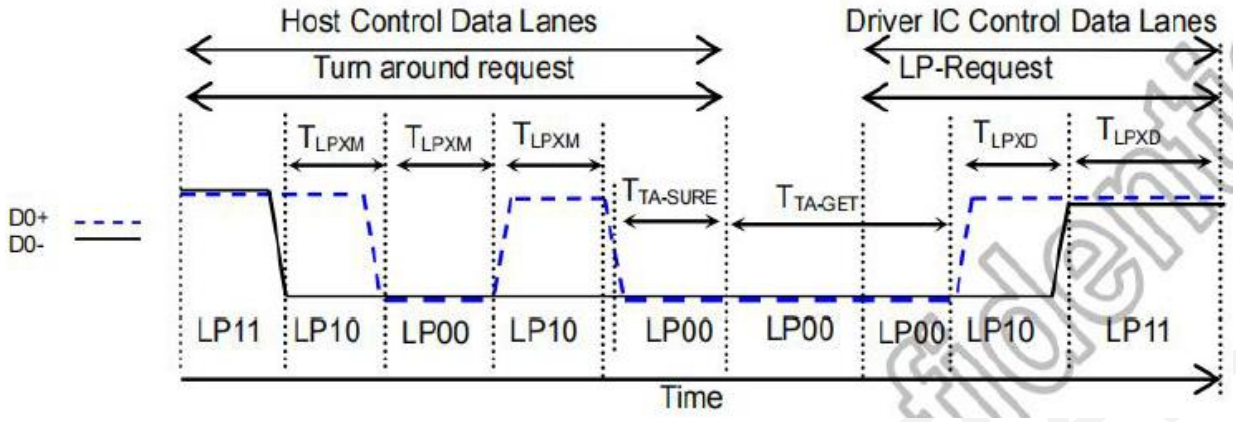


Figure: BTA from Display Module Timing to HOST

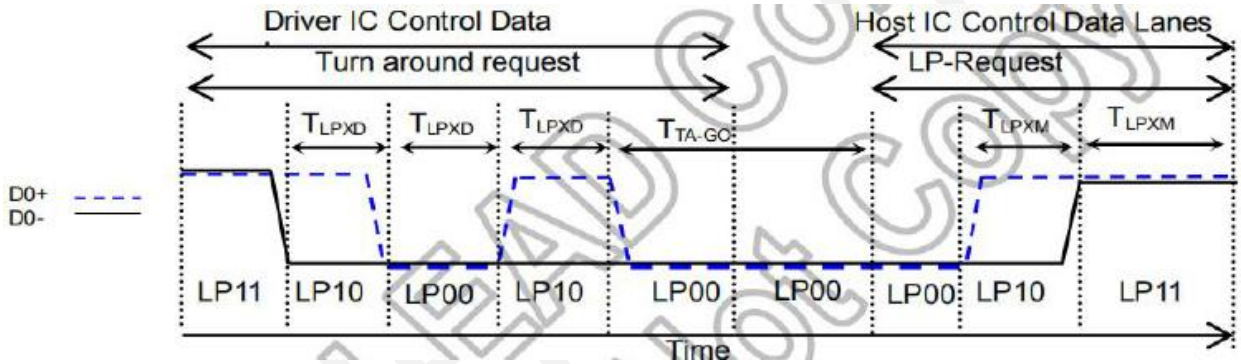


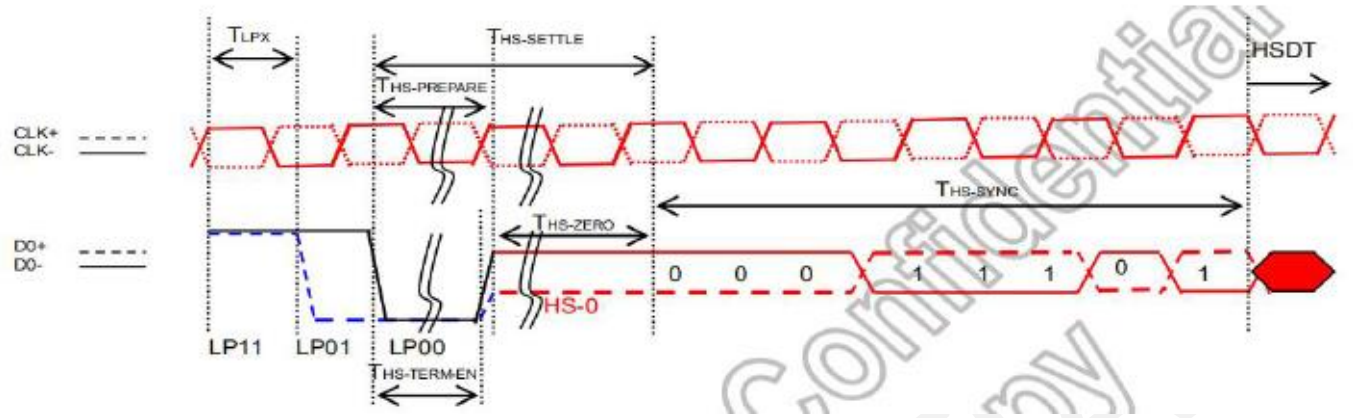
Table: DSI Low Power Mode Characteristics

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, TA=-30 to 70 ◦ C)

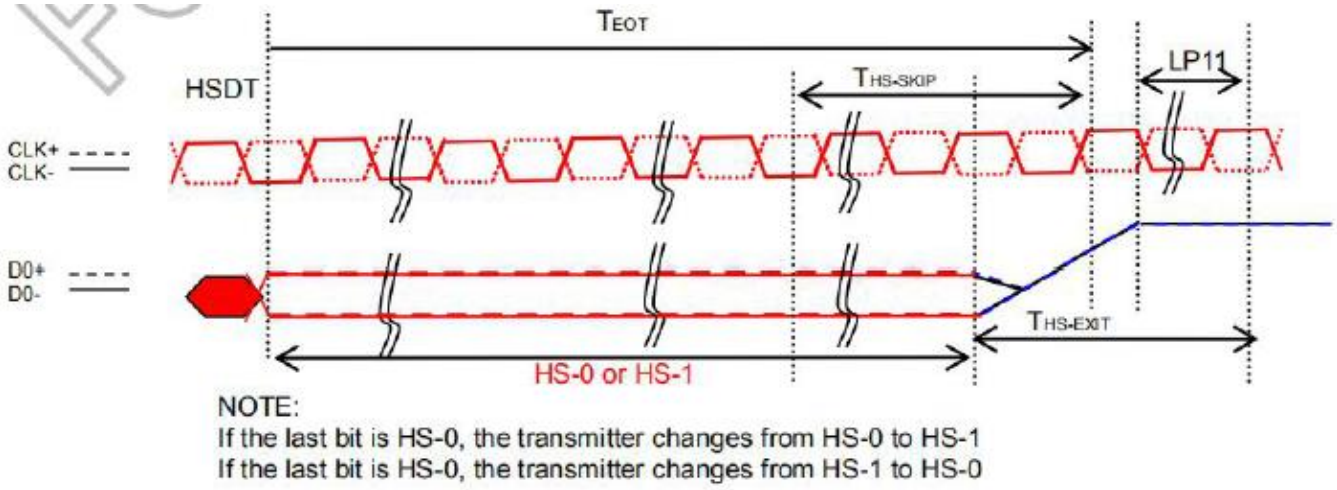
Signal	Item	Symbol	Min	Typ.	Max	Unit
DSI_D0P/DSI_D0P	Length of LP-00/LP01/LP10/LP11 Host→Display Module	T_{LPXM}	50	-	-	ns
	Length of LP-00/LP01/LP10/LP11 Display Module→ Host	T_{LPXD}	50	-	-	ns
	Time-out before the MPU start driver	$T_{TA-SURE}$	T_{LPXD}	-	$2xT_{LPXD}$	ns
	Time to drive LP-00 by display module	T_{TA-GET}	$5xT_{LPXD}$	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	$4xT_{LPXD}$	-	-	ns

3.5.2.3 Bursts

DSI Low Power Mode to High Speed Mode Timing



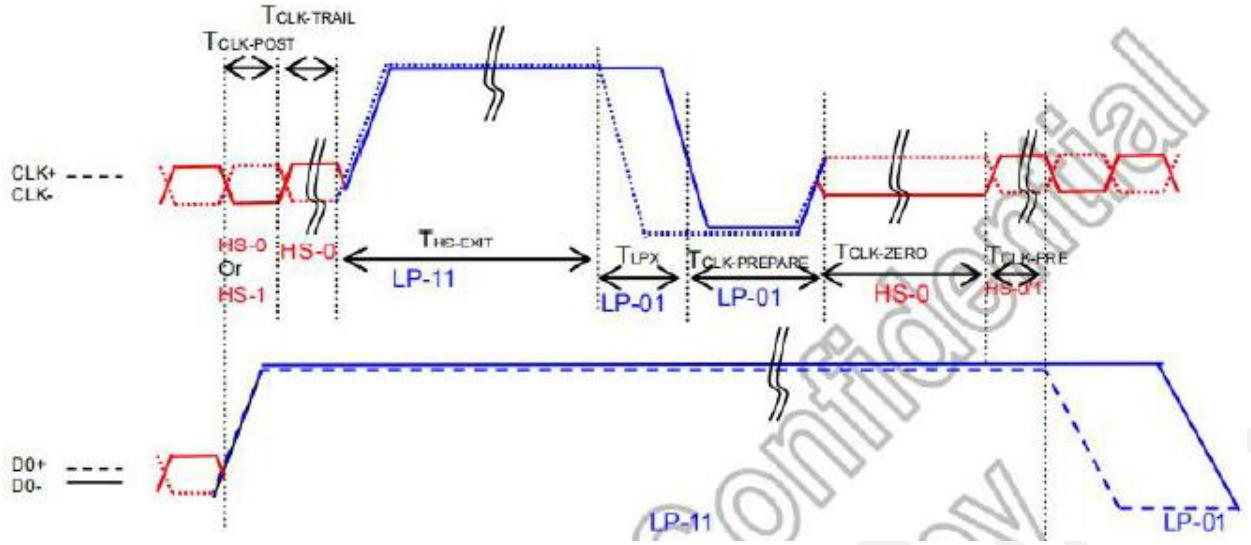
Signal	Item	Symbol	Min	Typ.	Max	Unit
DSI_D0P/DSI_D0P	Length of LP-00/LP01/LP10/LP11	T_{LPX}	50		-	ns
	Time to Driver LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI	-	85+6UI	ns
	Time to enable data receiver line termination	$T_{HS-TERM-EN}$	-	-	35+4xUI	ns
	Time to derive LP-00 by display module	T_{TA-GET}	$5xT_{LPXD}$	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	$4xT_{LPXD}$	-	-	ns



NOTE:
If the last bit is HS-0, the transmitter changes from HS-0 to HS-1
If the last bit is HS-0, the transmitter changes from HS-1 to HS-0

Signal	Item	Symbol	Min	Typ.	Max	Unit
DSI+D0P/DSI_D0P	Time-Out at Display Module to Ignore Transition Period of EoT	$T_{HS-SKIP}$	40	-	55+4xUI	ns
	Time to Driver LP-11 after HS Burst	TH_{S-EXIT}	100	-	-	ns

Clock Lanes High Speed Mode to/from Low Power Mode Timing



Signal	Item	Symbol	Min	Typ.	Max	Unit
DSI_CP/DSI_CN	Time that the MCU shall continue sending HS clock after the last associated Data Lane had transitioned to LP mode	$T_{CLK-POST}$	60+52xUI	-	-	ns
	Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60	-	-	ns
	Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100	-	-	ns
	Time to drive LP-00 to prepare for HS transmission	$T_{CLK-PREPARE}$	38	-	95	ns
	Time-out at Clock Lane Display Module to enable HS Termination	$T_{CLK-TERM-EN}$	-	-	38	ns
	Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}+T_{CLK-ZERO}$	300	-	-	ns
	Time that the HS clock shall be driven prior to any associated data Lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	8xUI	-	-	-

3.5.3 Reset Timing

Figure: Reset Input Timing

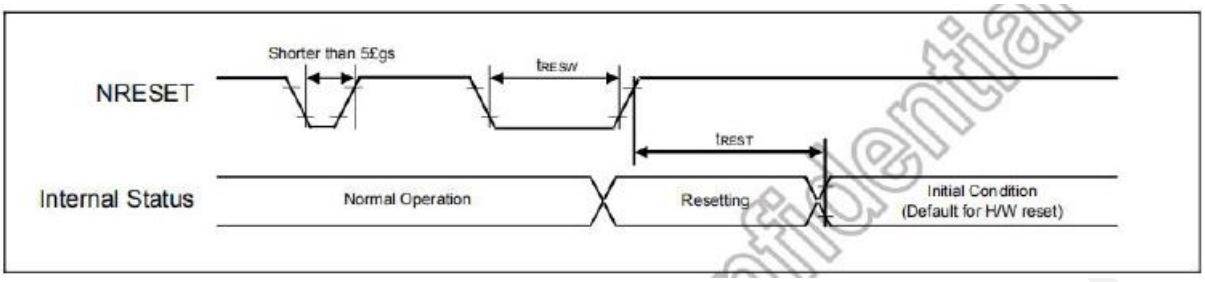


Table: Reset Input Timing

Symbol	Parameter	Related Pins	Min	Typ.	Max	Note	Unit
tRESW	Reset Low Pulse Width	NRESET	10	-	-	-	us
tREST	Reset Complete Time	-	15	-	-	When reset applied during SPLIN mode	ms
		-	120	-	-	When reset applied during SLPOUT mode	ms

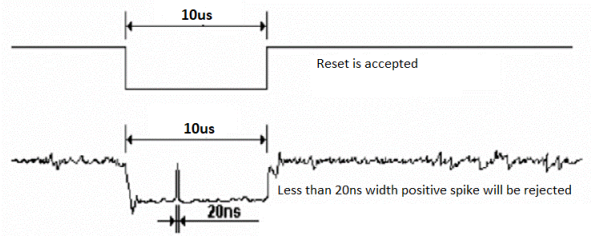
Note 1: Spike due to an electrostatic discharge on RESX line does not because irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset Start

Note 2: During the resetting period, the display will be blanked (the display is entering blanking sequence, which maximum time is 120ms, when reset starts in Sleep Out mode. The display remains the blank state in Sleep in mode) and then return to Default condition for Hardware Reset.

Note 3: During Reset Complete Time, ID and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) rising edge of NRESET.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5: It is necessary to wait 15msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

4. Electrical Specification Touch

4.1 Electrical Characteristics

4.1.1 Absolute Maximum Rating

Item	Symbol	Min	Max	Unit	Note
Power Supply Voltage	VDD	2.66	3.47	V	-
Operating Temperature	T_{OP}	-30	+85	℃	-
Storage Temperature	T_{ST}	-30	+85	℃	-

4.1.2 DC Electrical Characteristics (Ta=25℃)

(Ambient temperature:25℃, VDD=3.3V, VDDIO=1.8V or VDDIO=VDD)

Item	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	VDD	2.66	3.3	3.47	V	-
Normal mode operating current	-	-	8	14.5	mA	-
Green mode operating current	-	-	3.3	-	mA	-
Sleep mode operating current	-	70	-	120	uA	-
Doze mode operating current	-	-	0.78	-	mA	-
Digital input low voltage	VIL	-0.3	-	0.28*VDD	V	-
Digital Input high voltage	VIH	0.75*VDD	-	VDD+0.3	V	-
Digital output low voltage	VOL	-	-	0.15*VDD	V	-
Digital output high voltage	VOH	0.85*VDD	-	-	V	-

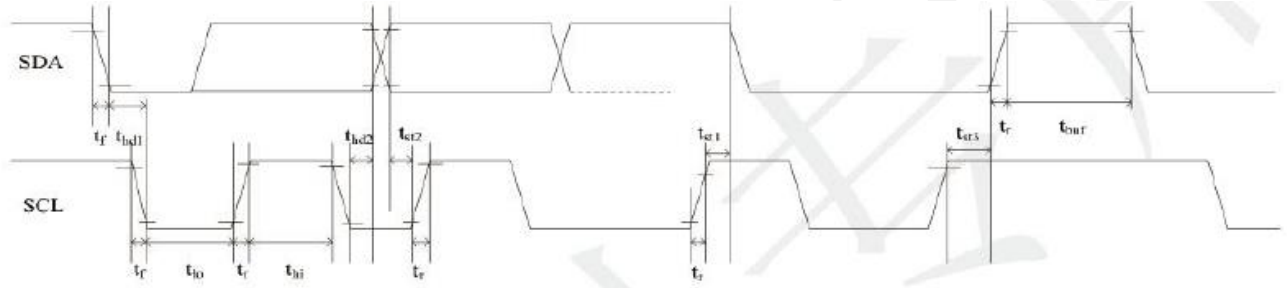
4.2 AC Characteristics

(Ambient temperature:25℃, VDD=2.8V, VDDIO=1.8V)

Item	Min	Typ.	Max	Unit	Note
SOC oscillation frequency	59	60	61	MHz	-
I/O output rise time, low to high	-	14	-	ns	-
I/O output rfall time, high to low	-	14	-	ns	-

4.2.1 I_2C Timing

GT911 provides a standard I2C interface for SCL and SDA to communicate with the host. GT911 always serves as slave device in the system with all communication being initialized by the host. It is strongly recommended that transmission rate be kept at or below 400Kbps. The I2C timing is shown below:



Test Condition: 1.8V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

Item	Symbol	Min	Max	Unit
SCL low period	tlo	1.3	-	us
SCL high period	thi	0.6	-	us
SCL setup time for Start condition	tst1	0.6	-	us
SCL setup time for Stop condition	tst3	0.6	-	us
SCL hold time for Start condition	thd1	0.6	-	us
SDA setup time	tst2	0.1	-	us
SDA hold time	thd2	0	-	us

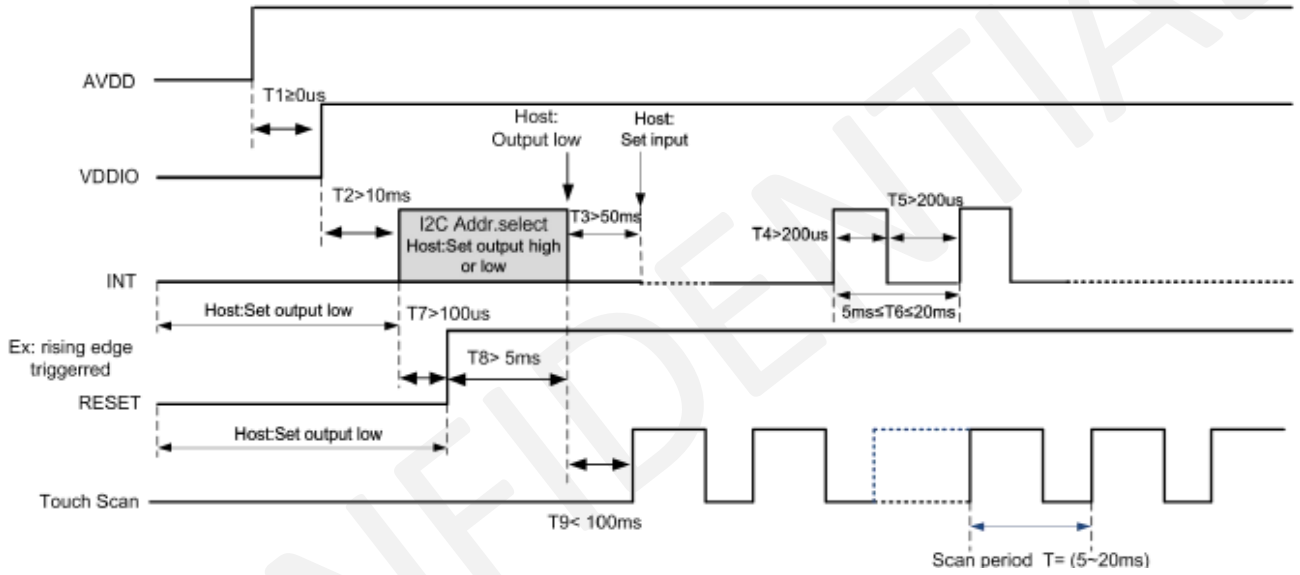
Test Condition: 3.3V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

Item	Symbol	Min	Max	Unit
SCL low period	tlo	1.3	-	us
SCL high period	thi	0.6	-	us
SCL setup time for Start condition	tst1	0.6	-	us
SCL setup time for Stop condition	tst3	0.6	-	us

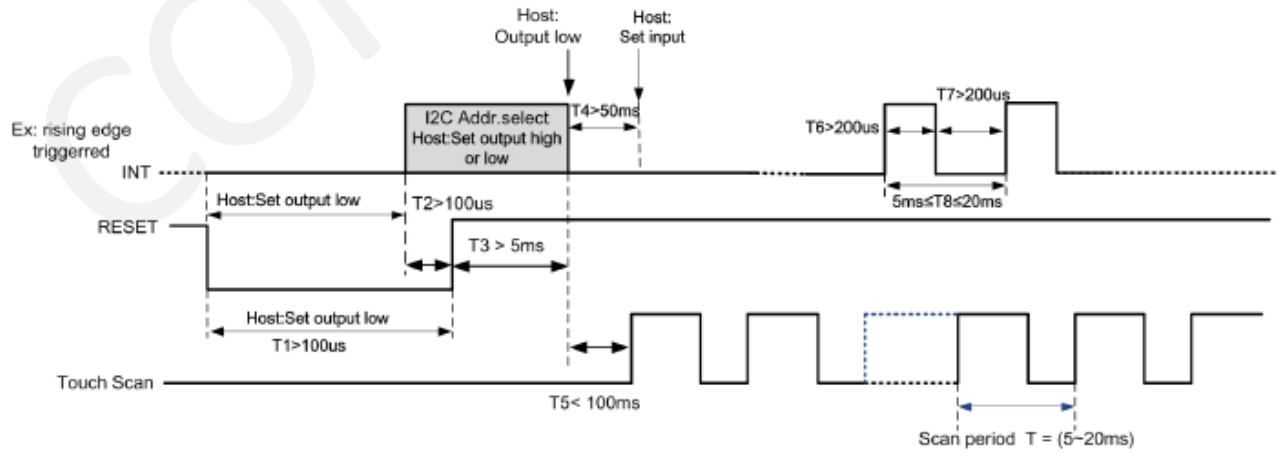
Item	Symbol	Min	Max	Unit
SCL hold time for Start condition	thd1	0.6	-	us
SDA setup time	tst2	0.1	-	us
SDA hold time	thd2	0	-	us

GT911 supports two I2C slave addresses: 0xBA/0xBB and 0x28/0x29. The host can select the address by changing the status of Reset and INT pins during the power-on initialization phase. See the diagram below for configuration methods and timings:

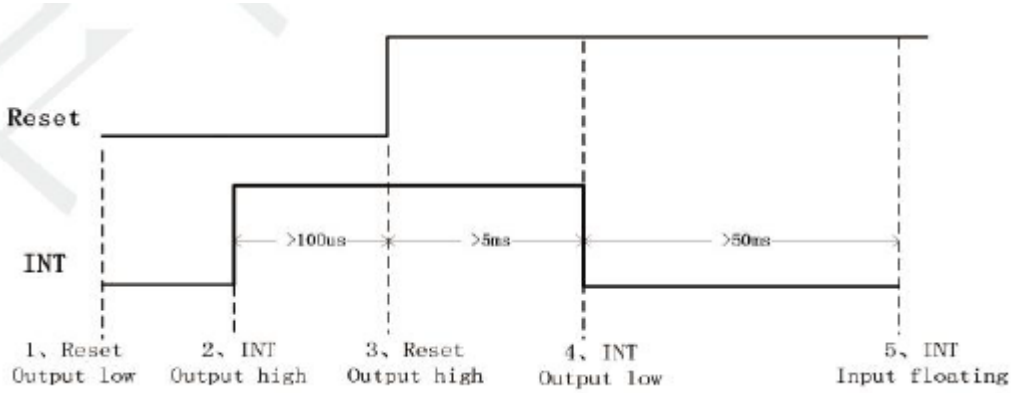
Power-on Timing:



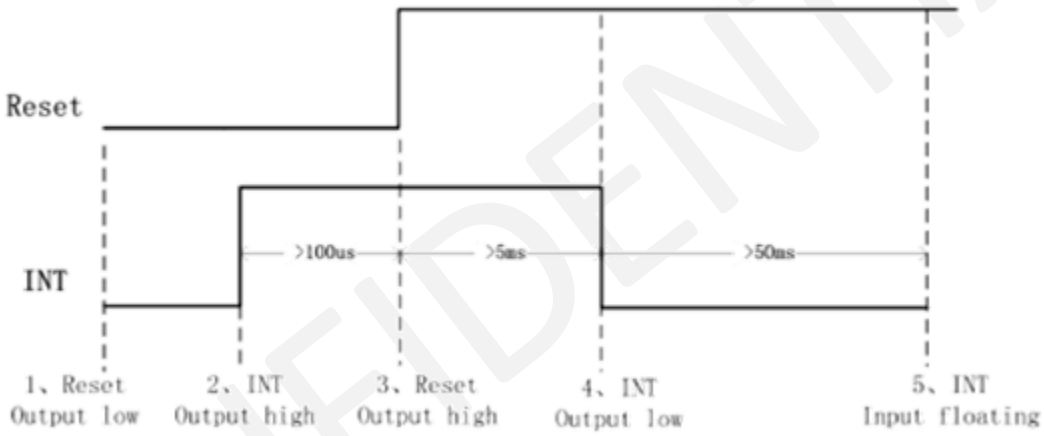
Timing for host resetting GT911:



Timing for setting slave address to 0x28/0x29:



Timing for setting slave address to 0xBA/0xBB:



a) Data Transmission

(For example：device address is 0xBA/0xBB)

Communication is always initiated by the host. Valid Start condition is signaled by pulling SDA line from “high” to “low” when SCL line is “high”. Data flow or address is transmitted after the Start condition.

All slave devices connected to I2C bus should detect the 8-bit address issued after Start condition and send the correct ACK. After receiving matching address, GT911 acknowledges by configuring SDA line as output port and pulling SDA line low during the ninth SCL cycle. When receiving unmatched address, namely, not 0XBA or 0XBB, GT911 will stay in an idle state.

For data bytes on SDA, each of 9 serial bits will be sent on nine SCL cycles. Each data byte consists of 8 valid data bits and one ACK or NACK bit sent by the recipient. The data transmission is valid when SCL line is “high”.

When communication is completed, the host will issue the STOP condition. Stop condition implies the transition of SDA line from “low” to “high” when SCL line is “high”.

b) Writing Data to GT911

(For example：device address is 0xBA/0xBB)

Figure: Timing for Write Operation

The diagram above displays the timing sequence of the host writing data onto GT911. First, the host issues a Start condition. Then, the host sends 0XBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where writing starts) and the 8-bit data bytes (to be written onto the register).

The location of the register address pointer will automatically add 1 after every Write Operation. Therefore, when the host needs to perform Write Operations on a group of registers of continuous addresses, it is able to write continuously.

The Write Operation is terminated when the host issues the Stop condition.

c) Reading Data from GT911

(For example：device address is 0xBA/0xBB)

Figure: Timing for Read Operation

The diagram above is the timing sequence of the host reading data from GT911. First, the host issues a Start condition and sends 0XBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where reading starts) to the slave device. Then the host sets register addresses which need to be read.

Also after receiving ACK, the host issues the Start condition once again and sends 0XBB (Read Operation). After receiving ACK, the host starts to read data.

GT911 also supports continuous Read Operation and, by default, reads data continuously. Whenever receiving a byte of data, the host sends an ACK signal indicating successful reception. After receiving the last byte of data, the host sends a NACK signal followed by a STOP condition which terminates communication.

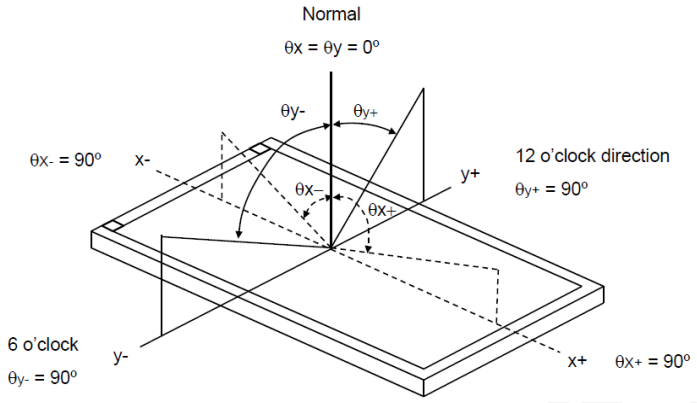
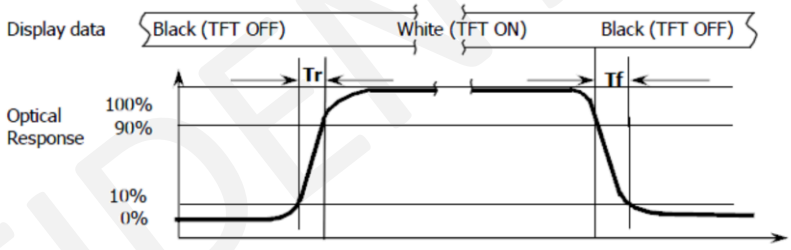
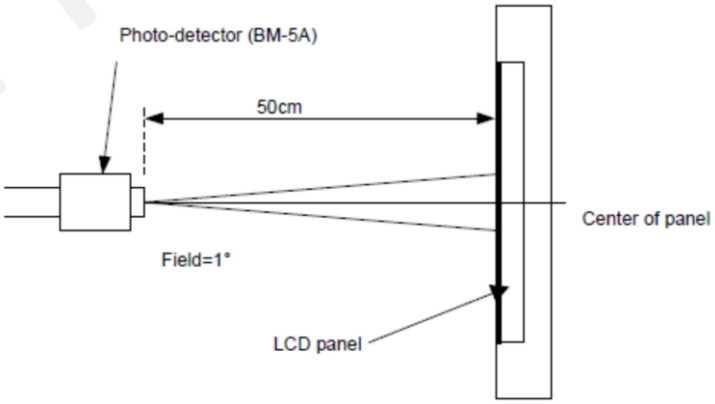
5. Optical Specification

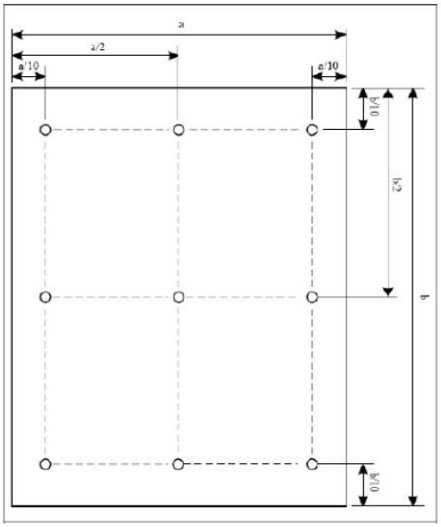
5.1 Optical Characteristics

Characteristics		Symbol	Conditions	Min	Typ.	Max	Unit	Note
Contrast Ratio		CR	θ = 0° Normal viewing angle	700	900	-	-	1, 2
Response time	Rising	TR + TF		-	25	35	msec	1, 3
	Falling							
Color Gamut		S(%)	-	55	60	-	%	-
Viewing Angle	Left	θ_x-	CR>10	80	85	-	-	1, 4
	Right	θ_x+		80	85	-		
	Up	θ_Y+		80	85	-		
	Down	θ_Y-		80	85	-		
Colour Chromaticity	Red	Rx	-	0.5830	0.6230	0.6630	-	1, 4 CA-310
		Ry		0.3117	0.3517	0.3917		
	Green	Gx		0.2703	0.3103	0.3503		
		Gy		0.5275	0.5675	0.6075		
	Blue	Bx		0.1076	0.1476	0.1876		
		By		0.0251	0.0651	0.1051		
	White	Wx		0.2656	0.3056	0.3456		
		Wy		0.3049	0.3449	0.3849		
Luminance		Lv	I_F = 40 mA	600	650	-	cd/m²	5
Uniformity		Avg	-	80	-	-	%	5

*The data comes from the LCD specification.

Note: Measuring Condition = in dark room, at ambient temperature 25±2℃, for 15 min, warm-up time.

Note	Item	Test method
1	Definition of Viewing Angle (θx, θy)	
2	Definition of Contrast Ratio (CR)	Measured at the center point of panel Contrast ratio (CR) = Luminance measured when LCD is at "white state" / Luminance measured when LCD is at "black state"
3	Definition of Response Time	
4	Definition of Optical Measurement Setup	

Note	Item	Test method
5	Definition of Luminance Uniformity	Luminance Uniformity of these 9 points is defined as below:  $\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$ $\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$

6. LED Backlight Specification

6.1 LED Backlight Characteristics

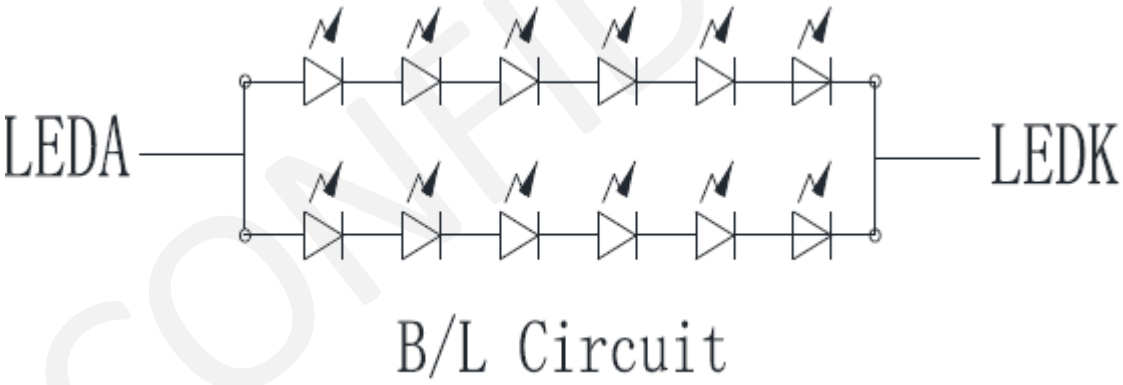
The backlight system is edge-lighting type with 12 chips LED.

Item	Symbol	Condition	Min	Typ.	Max	Unit	Note
Forward Current	I_F	-	35	40	-	mA	-
Forward Voltage	V_F	-	-	18.6	-	V	-
LED Life Time	Hr	-	-	50000	-	Hour	1, 2

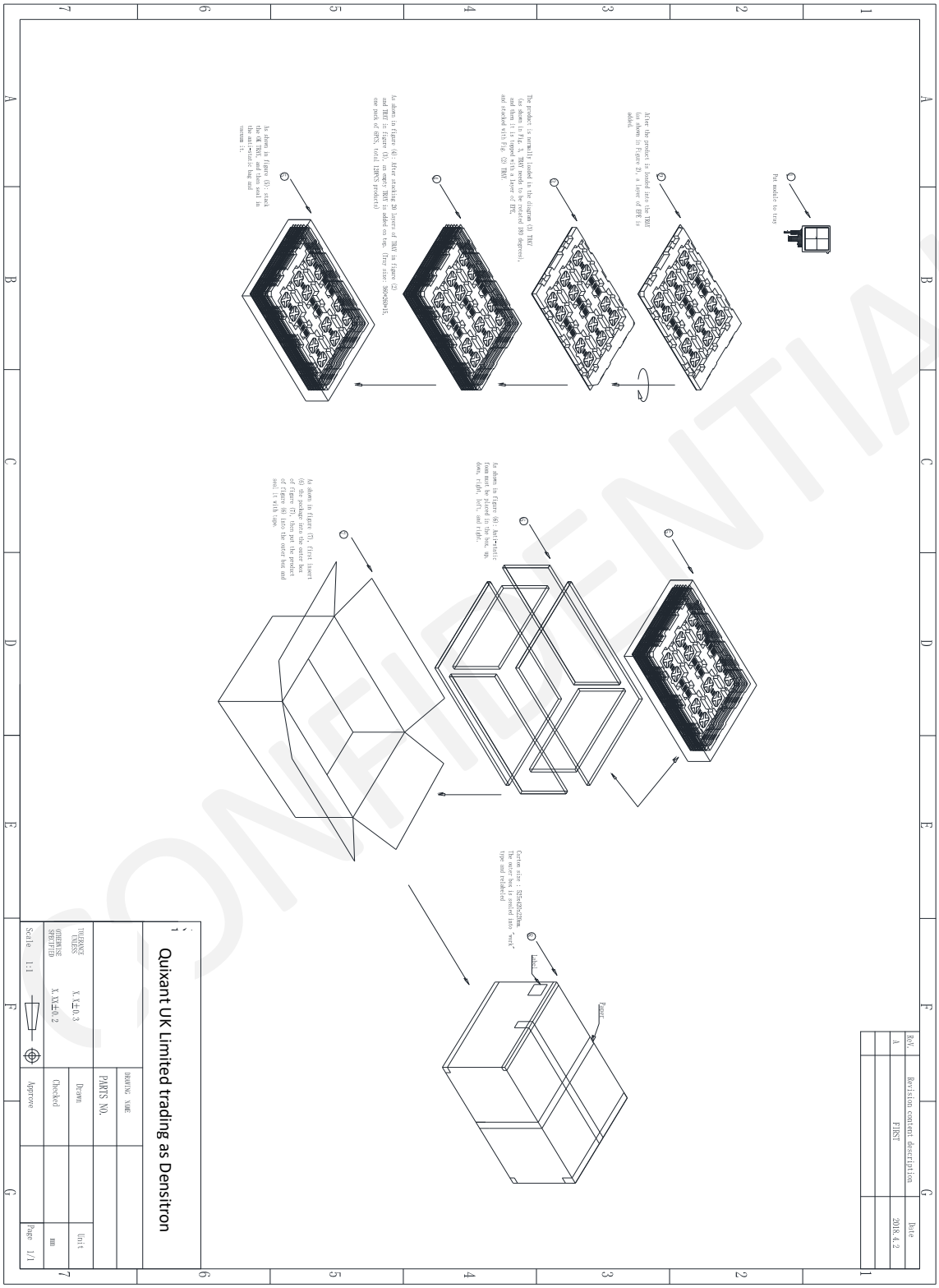
Note 1: LED Life Time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3℃, typical IL (I_F) value indicated in the above table until the brightness becomes less than 50%.

Note 2: The "LED Life Time" is defined as the module brightness decreases to 50% original brightness at Ta=25℃ and IL=40mA. The LED lifetime could be decreased if operating IL is larger than 40mA. The constant current driving method is suggested.

6.2 Internal Circuit Diagram



7. Packaging


Quixant UK Limited trading as Densitron
Rev
Revision content description
Date
A
FIRST
2018.4.2
Scale 1:1
Approve
Checked
Drawn
PARTS NO.
DRAWING NAME
Unit
mm
Page 1/1
CONFIDENTIAL

8. Quality Assurance Specification

8.1 Conformity

The performance, function and reliability of the shipped products conform to the Product Specification.

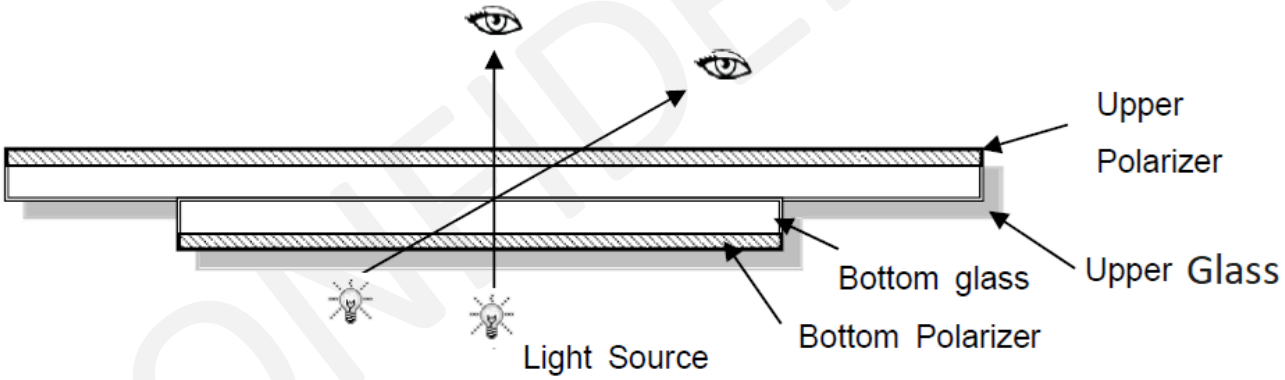
8.2 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	25 ± 5°C
Humidity:	65% ± 10% RH
Viewing Angle:	Normal Viewing Angle
Illumination:	Single fluorescent lamp (300 to 700 Lux)
Viewing distance:	30 - 50cm

Finger glove (or finger cover) must be worn by the inspector.

Inspection table or jig must be anti-electrostatic.

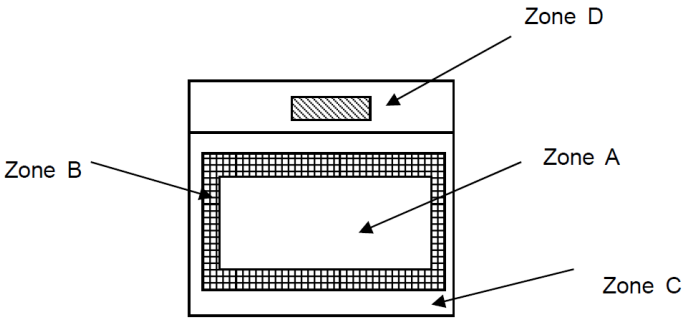


8.3 Delivery Assurance

8.3.1 Delivery Inspection Standards

Class II, Normal Inspection, MIL-STD-105E

8.3.2 Zone Definition



Zone A: Effective Viewing Area (Character or Digit can be seen)

Zone B: Viewing Area except Zone A

Zone C: Outside (Zone A + Zone B) Area which cannot be seen after assembly by customer.

Zone D: IC Bonding Area

Note: Generally, visual defects in Zone C can be ignored when it doesn't affect product function or appearance after assembly by customer

8.3.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.5	Defects in Cosmetic Check (Display Off)

LCD: Liquid Crystal Display, TP: Touch Panel, LCM: Liquid Crystal Module

No.	Items	Criteria	Classification of defects
1	Functional defects	1) No display, open or miss line 2) Display abnormally, short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component and etc.	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed.	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot Line defect	Light dot, Dim spot, (Note 1) Polarizer Air Bubble, Polarizer accidented spot and etc.	
6	Soldering Appearance	Good soldering, peeling off is not allowed.	
7	LCD/Polarizer/CTP	Black/White spot/line, scratch, crack, etc.	

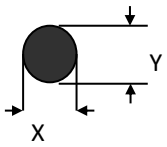
Note 1:

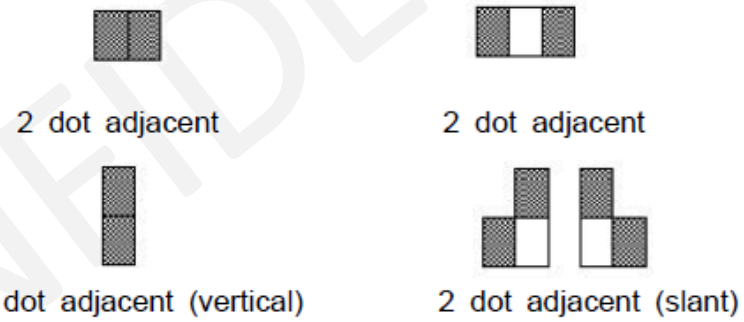
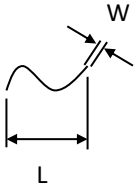
a) Light dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

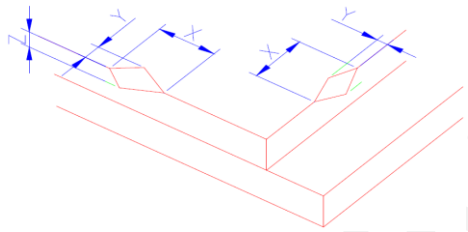
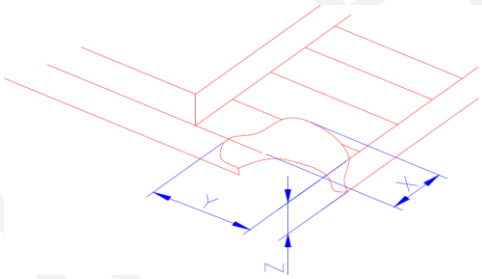
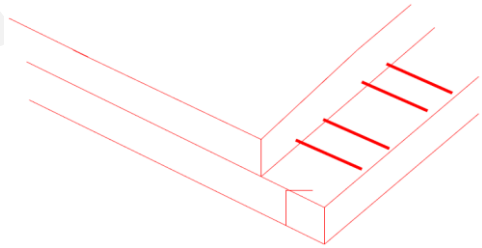
b) Dim dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

8.3.4 Criteria & Classification

Units: mm

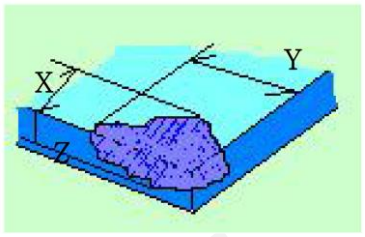
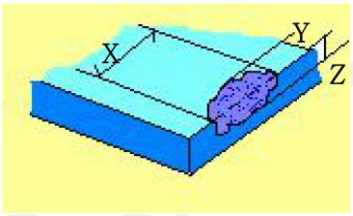
<table>
<tr><th>Class</th><th>Item</th><th colspan="5">Criteria</th></tr>
<tr><td rowspan="24">Minor</td><td rowspan="24">Spot Defect</td><td colspan="5">Round type: as per following drawing, ∅ = (X+Y)/2  </td></tr>
<tr><td colspan="5">1) Light Dot (Black/white spot, pinhole, stain, etc.)</td></tr>
<tr><td rowspan="2">Size\Zone</td><td colspan="3">Acceptable Quantity</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>∅≤0.15</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.15<∅≤0.25</td><td colspan="2">3(distance≧10mm)</td></tr>
<tr><td>0.25<∅≤0.40</td><td colspan="2">2(distance≧10mm)</td></tr>
<tr><td>0.4<∅</td><td colspan="2">0</td></tr>
<tr><td colspan="5">2) Dim Spot (Light leakage, dent, dark spot, etc.)</td></tr>
<tr><td rowspan="2">Size\Zone</td><td colspan="3">Acceptable Quantity</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>∅≤0.15</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.15<∅≤0.25</td><td colspan="2">3(distance≧10mm)</td></tr>
<tr><td>0.25<∅≤0.40</td><td colspan="2">2(distance≧10mm)</td></tr>
<tr><td>0.4<∅</td><td colspan="2">0</td></tr>
<tr><td colspan="5">3) Polarizer Accidented Spot</td></tr>
<tr><td rowspan="2">Size\Zone</td><td colspan="3">Acceptable Quantity</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>∅≤0.2</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.2<∅≤0.5</td><td colspan="2">2 (distance ≧ 10mm)</td></tr>
<tr><td>0.5<∅</td><td colspan="2">0</td></tr>
<tr><td colspan="5">4) Pixel Bad Points</td></tr>
<tr><td>Item</td><td>Zone A</td><td colspan="3">Acceptable Quantity</td></tr>
<tr><td rowspan="3">Bright Dot</td><td>Random</td><td colspan="3">N≤2</td></tr>
<tr><td>2 dots adjacent</td><td colspan="3">N≤0</td></tr>
<tr><td>3 dots adjacent</td><td colspan="3">N≤0</td></tr>
<tr><td>Dark Dot</td><td>Random</td><td colspan="3">N≤2</td></tr>
</table>

<table>
<tr><th>Class</th><th>Item</th><th colspan="4">Criteria</th></tr>
<tr><td rowspan="6"></td><td rowspan="6"></td><td rowspan="2"></td><td>2 dots adjacent</td><td colspan="2">N≤0</td></tr>
<tr><td>3 dots adjacent</td><td colspan="2">N≤0</td></tr>
<tr><td>Distance</td><td>1. Minimum Distance Between Bright dots.
2. Minimum Distance Between dark dots
3. Minimum Distance Between dark and bright dot.</td><td colspan="2">5mm</td></tr>
<tr><td colspan="2">Total bright and dark dot</td><td colspan="2">N≤4</td></tr>
<tr><td colspan="5">Note:
A) Bright dot：Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.
B) Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.
C) 2 dot adjacent = 1 pair = 2 dots
Picture:
 
2 dot adjacent　　2 dot adjacent
2 dot adjacent (vertical)　　2 dot adjacent (slant)</td></tr>
<tr><td colspan="5">5)　Polarizer Bubble</td></tr>
<tr><td rowspan="2">Size\Zone</td><td colspan="3">Acceptable Quantity</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>∅≤0.2</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.2<∅≤0.4</td><td colspan="2">3 (distance ≧ 10mm)</td></tr>
<tr><td>0.4<∅</td><td colspan="2">0</td></tr>
<tr><td rowspan="2">Minor</td><td rowspan="2">Line Defect (LCD/TP/ Polarizer backlight black/white line, scratch, stain)</td><td colspan="4">Line type: as per following drawing
 
</td></tr>
<tr><td></td><td>Length</td><td colspan="2">Acceptable quantity</td></tr>
</table>

<table>
<tr><th>Class</th><th>Item</th><th colspan="5">Criteria</th></tr>
<tr><td rowspan="5"></td><td rowspan="5"></td><td>Width</td><td></td><td>A</td><td>B</td><td>C</td></tr>
<tr><td>W≤0.05</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.05<W≤0.06</td><td>L ≤ 4.0</td><td colspan="2">N ≤ 3</td></tr>
<tr><td>0.06<W≤0.08</td><td>L ≤ 3.0</td><td colspan="2">N ≤ 2</td></tr>
<tr><td>0.08<W</td><td colspan="4">Define as spot defect</td></tr>
<tr><td>Minor</td><td>LCD
Crack/Broken</td><td colspan="5">Symbols:
X: Length, Y: Width, Z: Height, L: Length of ITO, T: Height of LCD
1) The edge of LCD broken: X≦3.0mm; Y<Inner border line of the seal; Z≦T
 
2) LCD corner broken: X≦3.0mm; Y≦L; Z≦T
  </td></tr>
<tr><td>Major</td><td>LCD Crack</td><td colspan="5">The LCD with extensive crack is not acceptable.
  </td></tr>
<tr><td>Major</td><td>Electronic
Components
SMT</td><td colspan="5">Not allow missing parts, solderless connection, cold solder joint, mismatch, The positive and negative polarity opposite</td></tr>
<tr><td>Minor</td><td>Display colour &
Brightness</td><td colspan="5">1) Colour: Measuring the colour coordinates in accordance with the datasheet or samples.</td></tr>
</table>

Class	Item	Criteria
		2) Brightness: Measuring the brightness of white screen in accordance with the datasheet or samples.
Minor	LCD Mura/Waving/ Hot Spot	Not visible through 5% ND filter in 50% gray or judge by limit sample if necessary.

Class	Item	Criteria				
Minor	CTP Related	1) CTP Cover Sensor Accidented Black/White Spot				
		Size\Zone	Acceptable Qty			
			A	B	C	
		∅≤0.1	Ignore		Ignore	
		0.1<∅≤0.2	3（distance≧10mm）			
		0.20<∅≤0.25	2（distance≧10mm）			
		0.25<∅	0			
		2) CTP Cover Scratch				
		Width	Length	Acceptable Qty		
				A	B	C
		Φ≤0.05	Ignore	Ignore		
		0.05<W≤0.06	L≤4.0	N≤3		
		0.06<W≤0.08	L≤3.0	N≤2		
		0.08<W	Define as spot defect			
		3) CTP Cover Pinhole / Lack of ink				
		Size\Zone	Acceptable Qty			
			C			
		∅≤0.1	Ignore			
		0.10<∅≤0.25	3 (distance ≧ 10mm)			
		0.25<∅≤0.30	2 (distance ≧ 10mm)			
		0.3<∅	0			
		4) CTP Bonding Bubble / Accidented Spot				
		Size\Zone	Acceptable Qty			
			A	B		
		∅≤0.1	Ignore			
		0.1<∅≤0.2	3 (distance≧10mm）			
		0.2<∅≤0.25	2 (distance≧10mm）			

Class	Item	Criteria	
		0.25<∅	0
		Assembly Deflection: beyond the edge of backlight ≤0.2mm	
Minor	CTP Related	TP cover broken X: length, Y: width, Z: height X≤0.5mm; Y≤0.5mm; Z<Cover thickness *Circuitry broken is not allowed.	
		TP cover broken X: length, Y: width, Z: height X≤0.3mm; Y≤0.3mm; Z<LCD thickness *Circuitry broken is not allowed.	

Criteria (functional items)

No.	Item	Criteria
1	No display	Not allowed
2	Missing segment	
3	Short	
4	Backlight no lighting	
5	CTP no function	

8.4 Dealing with Customer Complaints

8.4.1 Non-conforming Analysis

Purchaser should supply Densitron with detailed data of non-conforming sample.

After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.
If the analysis cannot be completed on time, Densitron must inform the purchaser.

8.4.2 Handling of Non-conforming Displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.
Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.
Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

9. Reliability Specification

9.1 Reliability Tests

Test Item	Test Condition	Evaluation and Assessment
High Temperature Operation	80℃,96H	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Non-display; 3.Missing segments/line; 4.Glass crack; 5.Current IDD is twice higher than initial value.
Low Temperature Operation	-30°C, 96 hrs	
High Temperature Storage	85°C, 96 hrs	
Low Temperature Storage	-30°C, 96 hrs	
High Temperature & High Humidity Storage	+60℃, 90％RH, 96HR	
Thermal Shock (Non-operation)	-10℃,30 min ↔ 60℃,30 min, Change time: 5min 20CYC.	
ESD test	C=150pF, R=330, 5points/panel Air: ±8KV, 5times; Contact: ±6KV, 5 times; (Environment: 15℃~35℃, 30%~60%).	
Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80cm (MEDIUM BOX)	

Note 1: The test samples should be applied to only one test item.

Note 2: Sample size for each test item is 5~10pcs.

Note 3: For Damp Proof Test, Pure water(Resistance ＞ 10MΩ) should be used.

Note 4: In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.

Note 5: Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

Note 6: The color fading mura of polarizing filter should not care.

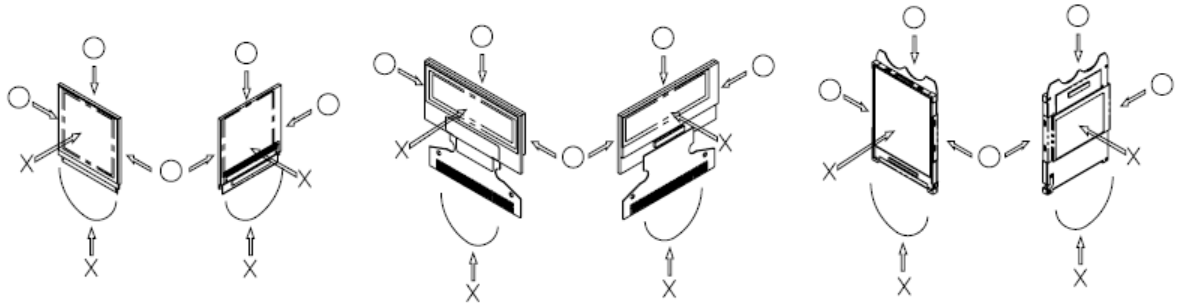
9.1.1 Inspection Check Standard

After the completion of the described reliability test, the samples are to be left at room temperature for 4 hrs prior to conducting the inspection check at 25±5 °C, 65±10% RH.

10. Handling Precautions

10.1 Handling Precautions

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water
4) If pressure is applied to the display surface or its neighbourhood of the display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
5) The polarizer covering the surface of the display module is soft and easily scratched. Please be careful when handling the display module.
6) When the surface of the polarizer of the display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   a. Scotch Mending Tape No. 810 or an equivalent
   b. Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.
   c. Also, pay attention that the following liquid and solvent may spoil the polarizer:
      - Water
      - Ketone
      - Aromatic Solvents
7) Hold the display module very carefully when placing it into the system housing. Do not apply excessive stress or pressure to display module. And, do not over bend the film with electrode pattern layouts. These stresses will



influence the display performance. Also, secure sufficient rigidity for the outer cases.
8) Do not apply stress to the LSI chips and the surrounding molded sections.
9) Do not disassemble nor modify the display module.
10) Do not apply input signals while the logic power is off.
11) Pay sufficient attention to the working environments when handing display modules to prevent occurrence of element breakage accidents by static electricity.

a. Be sure to make human body grounding when handling display modules.
b. Be sure to ground tools to use or assembly such as soldering irons.
c. To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
d. Protective film is being applied to the surface of the display panel of the display module. Be careful since static electricity may be generated when exfoliating the protective film.

12) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. If the display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
13) If electric current is applied when the display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

10.2 Storage Precautions

1) When storing display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps, etc. and, also, avoiding high temperature and high humidity environments or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Densitron) At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
2) If electric current is applied when water drops are adhering to the surface of the display module, when the display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

10.3 Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighbouring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the display module, fasten the external plastic housing section.
7) If power supply to the display module is forcibly shut down by such errors as taking out the main battery while the display panel is in operation, we cannot guarantee the quality of this display module.

10.4 Operation Precautions

1) It is indispensable to drive the display within the specified voltage limit since excessive voltage shortens its life.
2) Direct current causes an electrochemical reaction with remarkable deterioration of the display quality. Give careful consideration to prevent direct current during ON/OFF timing and during operation.
3) Response time is extremely delayed at temperatures lower than the operating temperature range while, at high temperatures, displays become dark. However, this phenomenon is reversible and does not mean a malfunction or a display that has been permanently damaged.
4) To protect display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the display modules.
   a. Pins and electrodes
   b. Pattern layouts such as the FPC
5) When the driver is being exposed (COG), semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if the driver is exposed to light, malfunctioning may occur.
   a. Design the product and installation method so that the driver may be shielded from light in actual usage.
   b. Design the product and installation method so that the driver may be shielded from light during the inspection processes.
6) Although the display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
7) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

10.5 Other Precautions

1) Request the qualified companies to handle industrial wastes when disposing of the display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.